coupled to the node. The ESD protection structure includes at least a single crystal Si resistor, which is formed over an insulating material layer and electrically coupled between the input pad and the node. The ESD protection structure further includes at least a single crystal Si-sided junction diode, which is formed over the insulating material layer and electrically coupled between one terminal of corresponding power supply and the node.

Discussion of Office Action Rejections

Applicants have cancelled claim 17 without disclaimer and prejudice.

Applicants have amended claims 1, 9, 14, and 21 to improve their clarity. No new matter adds by way of these amendments.

The Office Action rejected claims 1-21 under 35 U.S.C. 103(a), as being unpatentable over Yamaguchi et al. in view of Hu et al.. Applicants respectfully traverse the rejections for at least the reasons set forth below.

As shown in FIG. 3, there are at least two features to distinguish the present invention over the cited prior art references. The single crystal Si resistor 308 is horizontally isolated by the isolation structure 306. Also and the side junction diode is not a MOS diode, which is a MOS transistor but is operated as a diode. The side junction diode is clearly different from the MOS diode. It is clear that the MOS transistor include a gate oxide layer between gate and the substrate. However, a side junction diode includes no a gate electrode and the gate oxide layer below the gate electrode. The gate oxide layer has it specific function and is not generally equals to all kind of insulating layer.

With respect to independent claims 1 and 9, the resisting structure is recited in claims as follows:

> 1. An ESD protection structure having a single crystal Si-sided diode used to protect an internal circuit, the ESD protection structure electrically connected between an input pad and a node and the internal circuit electrically connected to the node, the ESD protection structure comprising:
>
> ***a single crystal Si resistor formed over an insulating material layer, electrically coupled between the input pad and the node, wherein the single crystal Si resistor is horizontally isolated by an isolation structure;*** and
>
> at least a single crystal silicon-sided junction diode formed over the insulating material layer, wherein the single crystal silicon-sided junction diode is electrically coupled between one terminal of a corresponding power supply and a node.
>
> 9. An ESD protection structure having a single crystal Si-sided diode used to protect an internal circuit formed from an insulating material layer on a SOI, the ESD protection structure electrically connected between an input pad and a node and the internal circuit electrically connected to the node, the ESD protection structure comprising:
>
> ***an input resistor including a plurality of single crystal resistors formed over the insulating material layer, wherein each of the single crystal resistors is electrically coupled between the input pad and the node, wherein the single crystal resistors are horizontally isolated by an isolation structure therebetween;*** and
>
> at least a single crystal sided junction diode formed over the insulating material layer, wherein the single crystal sided junction diode is electrically coupled between one terminal of a corresponding power supply and a node.

(*Emphasis added.*) The emphasized features in amended claims 1 and 9 about the resistors, which are specifically isolated by the insulating structure, are not disclosed by Yamaguchi et al. in view of Hu et al.

With respect to independent claims 14 and 21, they recite the feature of side junction diode as follows:

> 14. A semiconductor structure of ESD protection, the ESD protection electrically connects between an input pad and an integrated circuit, the semiconductor structure comprising:

a semiconductor substrate;

an insulating layer, formed on the semiconductor substrate;

at least a single crystal Si resistor, formed over the insulating layer;

at least a single crystal Si-sided junction diode, formed over the insulating layer, wherein the single crystal Si-sided junction diode does not includes a MOS transistor serving as a diode;

a first conductive layer, formed over the insulating layer, used to electrically connect one terminal of the single crystal Si resistor and the input;

a second conductive layer, formed over the insulating layer, used to electrically connect another terminal of the single crystal Si resistor and the integrated circuit; and

a third conductive layer, formed over the insulating layer, used to connect the single crystal Si-sided junction diode and the integrated circuit.

21. An ESD protection structure used to protect an internal circuit, the ESD protection structure electrically connected between an input pad and a node, and the internal circuit electrically connected to the node, the ESD protection structure comprising:

a single crystal Si resistor formed on an insulating material layer, electrically coupled between the input pad and the node; and

a single crystal layer formed on the insulating material layer, wherein the single crystal layer comprises at least two doped regions with different dopant type to form a side junction diode, and ***the side junction diode is electrically coupled between one terminal of a corresponding power supply and a node, wherein the side junction diode is not a MOS device that serves as a diode***.

(*Emphasis added.*) The features emphasized in independent claims 14 and 21 are also not disclosed by the prior art references.

In re Yamaguchi et al., even though Yamaguchi et al. disclose resistors in a circuit as shown in Fig. 19, Yamaguchi et al. failed to disclose how the resistor structure is formed. In Fig. 10, Yamaguchi et al. also disclose a resistor 64 which is separated by doped regions 61, 62 (col. 11, lines 1-11). When considering the invention as a whole, the resistors 308 formed on the insulating layer 302 and isolated by the insulation structure 306 is not specifically disclosed.

Moreover about the side junction diode, The Office Action refers to Fig. 22 to show a diode (39e +39c). However, as being previously discussed, the diode in Yamaguchi et al. is a MOS diode, which includes the gate oxide layer. The gate oxide layer is not to a general oxide layer.

The Office Action states "*The broad recitation of the claim does not preclude an oxide layer form being formed over the diode* (emphasis added)". The gate oxide layer is inherently existing in a MOS diode. Applicants have amended the claim to preclude the MOS diode. It is believed that the gate oxide layer is also precluded in the claims.

For at least the foregoing reasons, Applicants respectfully submits that independent claims 1, 9, 14, and 21 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-8, 10-13, 15-16, and 18-20 are patently define over the prior art references as well.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1-16 and 18-21 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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